Linearity vs. Power Consumption of CMOS LNAs in LTE Systems

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Abstract − This paper presents a study of linearity in wideband CMOS low noise amplifiers (LNA) and its relationship to power consumption in context of Long Term Evolution (LTE) system. Using proposed figure of merit to compare 35 state-of-the-art LNA circuits published in recent years, the paper shows a proportional but relatively weak dependence between amplifier performance (that is combined linearity, noise figure and gain) with power consumption. As a result, the predicted increase of LNA performance, necessary to satisfy stringent linearity specifications of LTE standard, may require a significant increase in power, a critical budget planning aspect for both handheld devices and base stations operating in small cells.

Keywords − LNA linearity, power consumption, LTE.

I INTRODUCTION

Long Term Evolution (LTE) is a next generation communication standard developed by 3GPP (3rd Generation Partnership Project) [1], allowing a high data rate transmission over radio interface. It represents a progression from voice transmission systems as GSM, through UMTS (with increased spectral efficiency for data transmission) to data transmission scheme where, majority of system throughput is used for high quality video streaming, internet access, file sharing and gaming, with peak downlink bandwidths in excess of 100 Mbps [2].

Such a dramatic increase in data throughput in relation to the older systems, corresponds to proportional increase in either a bandwidth (BW) or signal to noise ratio (SNR) or both at the same time. Both quantities can't be made arbitrary high. SNR is a function of maximum transmitted power allowed for the system, distance to the receiver and modulation scheme, and these parameters are usually optimised for the transmission. BW is controlled by the availability of a radio spectrum allocated for the system and, to certain extent, more bandwidth can be assigned to increase channel capacity if needed (providing that there is enough amount of unoccupied bandwidth left). Nowadays, the number of various wideband radio systems coexisting with LTE is significant and as a result, the radio spectrum has become relatively congested. 3GPP specified LTE frequency separation between frequency-division duplex (FDD) uplink and downlink is defined in the range of 45-400 MHz and even smaller distance to time-division duplex (TDD) transmission bands [1].

From a radio receiver perspective, relatively small frequency separation between bands requires improved selectivity in order to prevent unwanted signals to reach the receiver processing stages. Historically, the most practical has been the use of high selectivity pre-selection filters (more precisely duplexers in the transceiver) after the antenna, however in context of the wideband operation of LTE system, this approach becomes less practical. Since LTE transceivers operate in UHF band, 0.7-2.7 GHz (the range is not continuous), it is impossible to design a single RF pre-selection filter that is simultaneously wideband, has high roll-off characteristics and its centre frequency can be tuned to any band of interest.

When high performance wideband filter is not available, together with a wanted signal, radio receiver detects also unwanted components of the spectrum, in most cases having average power much larger than that of the signal of interest. This would not represent a serious problem if the receiver was a linear system (and not limited by maximum power supply voltages and currents), having ability to process signal of any strength with constant performance. In practice however, receiver subcircuits consist of number of transistors and the relationship between input and output is non-linear.

As a result, all of the unwanted signals in the receiver cross-modulate, with resulting products falling at wanted signal frequencies, dramatically reducing the effective SNR and transmission throughput. Non-linearity reduces gain of a wanted signal even further through two mechanisms known as *compression* and *blocking*, therefore further reducing SNR of received signal. Thus in order to mitigate problem of the destructive interference, special care has to be taken to design a receiver system with high linearity, especially in situations where a pre-selection filtering is far from ideal.

This paper explores linearity requirements of CMOS low noise amplifiers (LNA) in a context of LTE communication standard and in relation to the power consumption of the circuit. Linearity and power relationship is important not only for battery operating systems as handsets but also for base stations in femto-, pico- and metro-cells, operating with reduced power budget and multiple receivers. To our knowledge, a presented study on LTE linearity performance in relation to various CMOS LNA designs and its power budgets has not been conducted before.

Section II introduces fundamental aspects of circuit linearity together with a corresponding metrics. Section III shows linearity requirements for LTE receiver calculated from the system specification, whereas Section IV discusses its impact on both standalone LNA circuit and whole front-end design. Finally, Section V, introduces a figure of merit function for fair comparison of different published state-of-the-art CMOS LNA circuits and its relationship to power consumption. Also we formulate a prediction of relative power supply levels necessary for future designs of LTE-compatible integrated RF receiver front-ends.

II Amplifier Linearity Analysis

a) Taylor series description of soft non-linearity

As indicated in the previous section, circuits utilising transistors have in general a non-linear relationship between input and output. The main source of this behaviour are semiconductor materials which electrical properties are strongly dependant on electrical potential energy. In general, transistors can be used as switches and/or amplifiers (or more precisely transducers providing some form of proportional transformation between voltages and currents). When used as an amplifier, MOS transistor can be characterised by a soft non-linearity [3], that is, one can find a polynomial of a finite order, sufficiently describing the non-linearity for a limited range of input signal levels around certain bias point. In the simplest case, Taylor series can be used to define such polynomial, however when reactive components (transistor capacitances for example) become important, Volterra series approach should be used instead [3]. As an example, consider a simple low voltage LNA transconductance amplifier in common source (CS) configuration, biased using simple current mirror, depicted in Fig. 1. Inductors L_D and L_G have high impedance at frequency of interest, C_C are coupling capacitors providing DC isolation/RF short circuits to other stages connected to the LNA. Please note that for the following

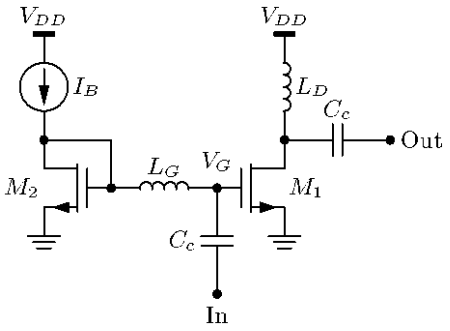

Fig. 1. Simple low voltage transconductance LNA.

linearity analysis we assume that impedance matching, noise figure and bandwidth are not critical. In practice all of these constraints have to be optimised simultaneously, which leads to a more complex circuit architecture. Output AC current of M_1 flowing through C_C can be described by the following polynomial:

$$i_o(t) = \sum_{k=1}^{\infty} g_k v_{in}^k(t) \approx \sum_{k=1}^{N} g_k v_{in}^k(t) \quad (2)$$

where g_k is *k-th* coefficient of the polynomial, defined as:

$$g_k = \frac{1}{k!}\frac{\partial^k i_{out}(V_0)}{\partial v^k} \quad (3)$$

that is, g_k represents *k-th* derivative of $i_o(t)$ in respect to the input voltage, for the device biased at certain DC point. Note that when the quiescent point of a soft non-linearity changes, the coefficients described by (3) have to be recalculated. In practice, the infinite series given by (2) is well approximated by the first 3 to 5 elements, as g_k is inversely proportional to factorial of k [3].

Polynomial description explains the effects of intermodulation, gain compression and blocking in non-linear radio receiver. Assuming that input voltage consists of two signals operating at different frequencies and g_2, $g_3 \neq 0$, using trigonometric identities, we can show:

$$v_{in}(t) = A \cdot \cos(\omega_1 t) + B \cdot \cos(\omega_2 t) \quad (4)$$

$$g_2 v_{in}^2(t) \propto g_2 AB \cdot \cos(\omega_1 t \pm \omega_2 t) \quad (5)$$

$$g_3 v_{in}^3(t) \propto \tfrac{3}{4} g_3 A^2 B \cdot \cos(2\omega_1 t \pm \omega_2 t) \quad (6)$$

$$g_3 v_{in}^3(t) \propto \tfrac{3}{4} g_3 A B^2 \cdot \cos(2\omega_2 t \pm \omega_1 t) \quad (7)$$

Thus, the output current (2) consists of many different sinusoidal components, where the ones given by (5) are the second order intermodulation products, IM2, whereas (6) and (7) are known as the third order intermodulation products, denoted IM3. Note that the magnitudes of IM2 and IM3 are proportional to A and B, and they increase much faster than the first order output terms given by:

$$i_{o1}(t) \approx \left(g_1 A + \tfrac{3}{4} g_3 A^3 + \tfrac{3}{2} g_3 A B^2\right) \cdot \cos(\omega_1 t) \quad (8)$$

$$i_{o2}(t) \approx \left(g_1 B + \tfrac{3}{4} g_3 B^3 + \tfrac{3}{2} g_3 B A^2\right) \cdot \cos(\omega_2 t) \quad (9)$$

Equations (8) and (9) show that the transconductor output at ω_1 and ω_2 depends on amplitudes of both signals. Interestingly, for $g_3<0$, the output current $i_o(t)$ is reduced by large amplitudes of wanted input signal (gain compression) and strong interference signal (known as blocking, AB^2 and BA^2 terms, respectively).

Formulas (5) - (9) allow us to introduce of a basic metrics for linearity analysis, known in a literature as *input intercept points* (IIP) [4,5]. As mentioned previously, IM products amplitude increases faster than the amplitude of fundamental signal, therefore it is possible to find theoretical input

amplitudes A and B for which the resulting IM products would level with the fundamental. The second order (IIP2) and third order (IIP3) intercept points are respectively defined as [4,5]:

$$IIP_2 = \left|\frac{g_1}{g_2}\right| \tag{10}$$

$$IIP_3 = \sqrt{\frac{4}{3}\left|\frac{g1}{g3}\right|} \tag{11}$$

In practice, values for IIP2 and IIP3 are typically much larger than the maximum voltages and currents allowed in the circuit, and are approximated by finding a crossover points of tangent lines from measurements of IM2, IM3 and fundamental responses. The higher the IIP2 and IIP3 magnitudes, the better performance from linearity perspective is.

b) IIP2 and IIP3 analysis example

As an example, consider large signal UMC 130 nm NMOS RF transistor model (L=0.12 µm, W=0.9 µm, NF=4, M=1, V_{DD}=1.2 V) employed in the LNA circuit from Figure 1. Polynomial coefficients (3) as function of gate bias voltage *VG* were obtained using Eldo RF circuit simulator. Using (10) and (11) we can calculate IIP2 and IIP3 for the amplifier. The results are depicted in Fig. 2. Note that both intercept points are given in terms of power referred to 50 Ω, which is a standard notation throughout RF literature. The presented curves show that there are three possible bias points for improved linearity, where IIP2 and IIP3 are at their respective maximums:

- VG≈420 mV, ID=87 µA, gm=1.19 mA/V, PDC= 0.104 mW, IIP2≈4.5 dBm, IIP3≈30 dBm.
  At this point IM3 products are minimised as well as a power consumption. Transistor is biased where $g_{3\approx}0$, resulting in high IIP3. IM2 products are not minimised, but they are usually not a limiting factor for a linearity performance of the receiver when originate from LNA (IIP2 becomes crucial for mixers) [4,5]. However, at this bias point, small *gm* translates into reduced gain and from a noise perspective, this has a negative impact on system SNR. Since unity gain frequency f_t of the transistor is proportional to *gm* a maximum operation frequency of the circuit can be limited as well.
- VG≈1080 mV, ID=1.87 mA, gm=3.17 mA/V, PDC= 2.24 mW, IIP2≈45 dBm, IIP3≈20 dBm.
  At this point IM2 products are minimised, IM3 products are relatively small as well. The transconductance is at its maximum, 2.6 times larger than in the previous case, improving both gain and f_t. The cost however is more than 20 times more power dissipated by the transistor than before.
- VG≈700 mV, ID=0.71 mA, gm=2.86 mA/V, PDC= 0.85 mW, IIP2≈13 dBm, IIP3≈13 dBm.
  Depending on the system requirements (discussed in detail later in this paper), this point may represent a design trade-off between power consumption and linearity, delivering 90% of maximum gain with more than a 60% of power reduction in comparison to the previous case.

As mentioned before, in practice the design of LNA has to involve a simultaneous optimisation of noise, impedance matching, gain, stability and linearity (as all of these can't be maximised at the same time), however the presented methodology can be used as a starting point for a linear LNA design with a limited power budget.

In practice the linearity of LNA can be improved by means of feedback techniques, without additional power consumption (as passive RLC components are used for this purpose), however this solution is not always feasible at RF frequencies, and therefore some other methods like feed-forward or post-distortion cancellation have to be used, for the cost of higher power consumption [6]. Therefore, in general LNA linearity and power relationship is not as straightforward as one could expect (more details are presented in Section V).

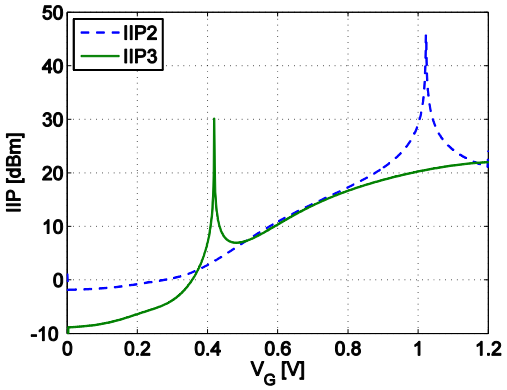

Fig. 2. IIP2 and IIP3 of the amplifier from Fig. 1.

III LTE Linearity Requirements

a) 3GPP LTE specification and system parameters

The linearity requirements for LTE are not reported specifically by 3GPP, however after some elaboration they can be derived from the intermodulation specifications 36.101 and 36.104 [1] for both user equipment (UE) and base station (BS) receivers, respectively. In this paper we use the most recent version of aforementioned LTE specification, Revision 11, March 2013 and we limit our calculations to UE, as BS has more scenarios differing in performance (namely: Wide Area, Medium Range, Local Area and Home). However, the presented formulation can be successfully applied to any type of BS if necessary. In order to represent performance variations in different propagation scenarios, 3GPP considers reference carriers with QPSK, 16QAM and 64QAM modulations, and following bandwidths: 1.4, 3, 5, 10, 15 and 20 MHz. In this work we present calculations for QPSK case for all bandwidths and for a single LTE Band 2 (uplink, UL, centred 1960 at MHz, downlink, DL, at 1880 MHz, 60 MHz bandwidth, 80 MHz separation) [2]. Finally, as mentioned previously, we will focus only on IIP3 as, assuming that the second order distortion in LNA is not usually a limiting factor for the linearity of complete receiver. All system parameters necessary to calculate IIP3 are presented in Table 1:

- $P_{REFSENS}$ is a minimum average power applied to UE antenna ports (LTE assumes 2 Rx antennae for

diversity scheme) to achieve at least 95% of maximum throughput.

- Thermal noise floor for given bandwidth at temperature of 290K.
- *Rx Margin* is a required increase in minimum average received signal power in the presence of blockers and interferers over nominal $P_{REFSENS}$ value.
- 3GPP derives intermodulation requirements for two interfering signals, one is a continuous wave (CW), the other one is a modulated carrier with bandwidth ranging in between 1.4-5 MHz.

Tab. 1. LTE sensitivity and noise parameters for Band 2

Param.	Bandwidth [MHz]					
	1.4	3	5	10	15	20
$P_{REFSENS}$ [dBm]	-103	-100	-98	-95	-93	-92
Noise floor [dBm]	-113	-109	-107	-104	-102	-101
Rx Margin [dB]	12	9	6	6	7	9
Int BW [MHz]	1.4	3	5			

c) In-band IIP3 specification

In-band linearity requirement defines a receiver robustness against cross-modulation products of other channels of the same band or any CW interferer present within the band of interest. According to 36.101 rev.11 specification, the receiver has to be able to detect a wanted signal in a presence of two interferers with average power of -46 dBm each. CW interferer is placed at -BW/2-7.5 MHz (low side) or BW/2+7.5 MHz (high side) from the carrier frequency of the band of interest, whereas the modulated interferer is located at twice the frequency of the CW signal. For example, considering high side interferers and BW of a wanted signal of 10 MHz, the CW interferer is located at 12.5 MHz from the carrier, whereas 5 MHz modulated interferer is 25 MHz above the carrier. It is easy to show that one of their IM3 products at $2f_{CW}$-f_{IM} is centred around the carrier as well:

$$f_{IM3} = 2(f_c + 12.5\ MHz) - (f_c + 25\ MHz) = f_c \qquad (12)$$

Assuming that the intermodulation products are allowed to increase noise floor from Table 1 by *Rx Margin*, that for 10 MHz signal bandwidth is equal to 6 dB, resulting in maximum noise floor of -98 dBm. Since thermal noise and IM3 products are not correlated, we can calculate the maximum power of intermodulation components:

$$P_{IM3} = 10\log_{10}\left(10^{-\frac{98}{10}} - 10^{-\frac{104}{10}}\right) = -99.26\ dBm \qquad (13)$$

As the interferer bandwidth is 5 MHz for the considered case, IM3 product occupies exactly half of the signal BW. Thus, (13) has to be corrected by the ratio of two quantities, which now represents an equivalent average IM level for 10 MHz wanted signal [7]:

$$P_{IM3} = -99.26 - 10\log_{10}\left(\frac{10\ MHz}{5\ MHz}\right) = -102.24\ dBm \qquad (14)$$

Finally, IIP3 can be estimated taking power of interferers and calculated power of the third order intermodulation product [8]:

$$IIP3 = 0.5(3P_{INT} - P_{IM3}) = 0.5(-46 \cdot 3 + 102.24) = \qquad (15)$$
$$= -17.88\ dBm$$

Table 2 presents the results of in-band IIP3 calculations for all the possible BW values. Note that our calculations are 3-4 dB more stringent to the results of Sesia et al. [7], where the authors used an average implementation margin of 2.5 dB in their calculation, but did not provide any explanation behind this choice. Thus, we assumed that in practice more margin may be necessary, for example due to process variations.

Tab. 2. Calculated IIP3 for LTE assuming two -46 dBm interferers (in-band) and -31 dBm interference (out-of-band).

BW	P_{IM3}	In-band IIP3	Out-of band IIP3
[MHz]	[dBm]	[dBm]	[dBm]
1.4	-101.28	-18.36	+4.19
3	-100.58	-18.71	+3.84
5	-102.24	-17.88	+4.68
10	-102.24	-17.88	+4.68
15	-100.74	-18.63	+3.92
20	-98.59	-19.70	+2.85

d) Out-of-band IIP3 specification

Due to a limited performance of receiver pre-selection filters and finite isolation of duplexer in radio transceiver, strong signals from the transmitter side are injected into the receiver. This is chiefly a problem for FDD system, where the transmitter and receiver are operating simultaneously. Taking a maximum average power of LTE signal from the transmitter output of +24 dBm, a typical duplexer isolation of 50 dB , and 2 dB losses in the receive path [7], interferer as strong as -28 dBm can reach the receiver. If a strong CW signal falls between Rx and Tx bands (namely at half the duplex distance) IM3 products will fall into the band of interest.

As previously, IIP3 specification is reported directly by 3GPP however it can be derived from out-of-band blocking requirements [7,8]. The maximum power of CW interferer depends on its distance from the edge of a wanted band, and is respectively (in reference to the upper limit): -44dBm from 15 MHz to 60 MHz, -30 dBm from 60 MHz to 85 MHz and -15 dBm above 85 MHz offset [1]. For Band 2 considered in this paper, the duplex separation is equal to 80 MHz, thus a -44 dBm CW interferer at 40 MHz offset from the received band cross-modulates with the transmitter leakage. As Band 2 has a

relatively wide UL and DL bandwidths in relation to the duplex distance (60 MHz vs 80 MHz), the resulting filtering of CW between bands will be limited. As an example consider a commercially available Band 2 duplexer from Avago Tech., ACMD-7410, that provides approx. 4 dB attenuation at CW frequency [9]. Thus, interferer of -48 dBm has to be considered.

As both CW and the leakage signal power in relation to the receive band are strong functions of duplexer transfer function, Sesia et al. [7] suggests using an average interference power to calculate IIP3. In the presented example, the average power of the interference from -28 dBm leakage and -48 dBm CW is equal to -31 dBm. Using (15) and assuming allowed power of IM3 products from (13) and (14), the resulting out-of-band IIP3 values are presented in Table 2.

It can be seen that the out-of-band requirement is much more stringent than in the case of in-band calculation (-17 dBm against +5 dBm). In the case of the former, a duplexer specification determines the linear performance of the receiver (this is the most likely why 3GPP does not define IIP3). In the case of stronger interferers and limited filtering in wideband applications, this leads to further increase in out-of-band IIP3 levels.

IV Amplifier vs. LTE Front-End Linearity

In order to show how system level linearity translates to IIP requirements of LNA, let us consider a simplified model of cascaded RF heterodyne front-end, depicted in Fig. 3. The system consists of an LNA, followed by a mixer and intermediate frequency (IF) amplifier. Each block is described by the power gain as well as IIP3. We assume that all blocks are impedance matched, which in practice is valid only for a limited range of frequencies. For clarity, any inter-stage filters were omitted, assuming that at frequency of interest they introduce negligible insertion loss and their respective IIP3 levels are relatively high.

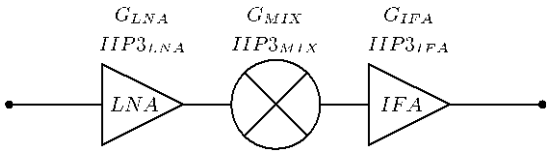

Fig. 3. RF front-end cascade: LNA, mixer and IF amplifer.

Well known approximation of 3 stage cascade from Fig. 3, is given by [4,5]:

$$\frac{1}{IIP3_{tot}} \approx \frac{1}{IIP3_{LNA}} + \frac{G_{LNA}}{IIP3_{MIX}} + \frac{G_{LNA}G_{MIX}}{IIP3_{IFA}} \qquad (16)$$

Where, G represents power gain and IIP3 is power referred to a characteristic impedance common for all the blocks. Although simple, (16) allows us to analyse how LNA affects the performance of the cascade. The rule of thumb is that the linearity of the cascade is defined by the last stage (IF amplifier in Fig. 3) as its IIP3 is scaled down by the total gain of previous stages. This is generally true assuming that linearity of LNA and mixer *are not a limiting factors*. In practice however, in order to provide wide bandwidth, constant gain and low noise figure, linearity of the LNA can't be designed arbitrarily high. In addition, in order to reduce front-end power consumption, improve noise figure and linearity, a passive mixer with negative conversion gain can be used. Thus, the more detailed analysis is necessary. As an example consider a typical IF amplifier with power gain of 20 dB and IIP3 in the range of 25 to 30 dBm [10]. Assuming a constant gain of the LNA and passive mixer, equal to 15 dB and -6 dB respectively, we can show that the total IIP3 of the cascade from (16) is strongly dependent on both intercept point levels of LNA and mixer. Fig. 4. depicts the results of total IIP3 calculation as a function of LNA linearity for the parametric sweep of mixer third order intercept point. Dashed line represents a +5dBm IIP3 target corresponding to LTE out-of-band specification calculated in Section III.

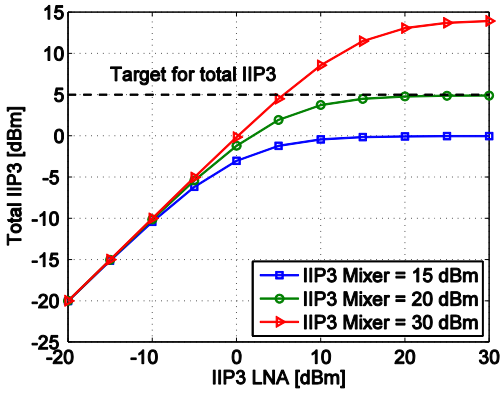

Fig. 4. IIP3 of the cascade vs. IIP3 of LNA.

It can be seen that for low values of LNA IIP3 (<<0 dBm), the amplifier limits the linearity of the cascade. The curves start to diverge strongly where LNA IIP3 reaches 0 dBm. At this point the mixer intercept point is reduced by the LNA gain and becomes the dominant factor. Finally, a highly linear LNA has no effect on the total IIP3 of the cascade, now controlled fully by the intermodulation performance of the mixer. Thus, in order to achieve out-of-band IIP3 performance of the LTE system, it is critical to use both highly linear mixer and LNA combinations. Providing that a typical RF passive mixers in discrete implementations achieve IIP3 in the range of 25 to 35 dBm [10], a rough estimation of intercept point for LNA operating in LTE receiver yields +5 dBm. In practice, we should expect limited performance due to impedance mismatches, non-uniform gain changing with frequency and non-ideal duplexer transfer function. It is therefore safe to assume that IIP3 of +10 dBm is more realistic target for LTE wideband low noise amplifier.

V Prediction of LNA Power Consumption In Context of LTE Systems - Results

This section presents the results of performance comparison of 35 different CMOS wideband LNA circuits published in recent years (Tab. 3, on a separate page) [11-46]. To allow fair comparison, every circuit is characterised by power gain (G, dB), noise figure (NF, dB), minimum and maximum frequency of operation (f_{min} and f_{max} respectively, MHz), fractional bandwidth (FBW), IIP3 (dBm) and DC power (P_{DC}, mW). Note that some of the published circuits use a voltage gain in

place of power gain. In order to follow system level design standards, we translated gain of all LNAs into power domain. It is assumed that the DC power consumption is referred to LNA core, as many of the authors do not report it explicitly. Fractional bandwidth follows a standard RF definition of a ratio of difference between f_{max} and f_{min} to the centre frequency between the two. In cases where G and NF were varying over the band of interest, the best of the reported values was chosen.

In order to show that a relationship between linearity of RF LNA and DC power is not straightforward, consider the results of IIP3 comparison, depicted in Fig. 5. Dots correspond to the third order intercept points from Tab. 3, whereas the solid line represents a linear trend calculated on the dataset. It can be seen that IIP3 is weakly dependent on power consumption (+0.06 dB/mW). Counterintuitive at first, this behaviour is expected. As indicated previously in Section II, power increase can help to reduce intermodulation effects in simple LNAs, however it may not necessarily yield the best noise, impedance matching and stability performance. Therefore, in order to improve other design constraints, linearity and power have to be traded-off, resulting in the constant trend from Fig. 5. For example, in comparison with other circuits, two LNAs with the highest linearity have either relatively low fractional bandwidth [21], or high noise figure [32]. Note that among the reported state of the art CMOS LNAs, only the two described topologies meet IIP3 requirement from Section III.

In order to include effects of gain, noise and linearity, figure of merit (FoM) function has to be used. Usually the DC power consumption contributes to total FoM, however in order to analyse the performance of LNA as a function of the power, we calculate FoM without power :

$$FoM_{w/oP}[dBm] = G + IIP3 + 10\log_{10}(FBW) - NF \quad (17)$$

Note that all of the elements in (17) contribute equally to the total FoM, thus a high performance LNA is characterised by minimum noise, wide tuning range, high gain and IIP3, resulting in proportionally high FoM values.

Fig. 6 depicts the results of FoM calculation. As before, dots represent the data points from Tab. 3, whereas solid line is a linear trend. The average FoM is equal to 26.8 dBm, with average power consumption of 18.3 mW. It can be seen that higher FoM requires more DC power, which confirms our assumption that optimised wideband LNA consumes more energy. Note that this relationship is not strong as the slope of a trend line is approx. +0.19 dB/mW. In order to increase FoM of CMOS LNA by 3 dB, a corresponding increase in power of 16 mW is necessary. Assuming IIP3 of +10 dBm as a target for LTE LNA (derived in Section IV), together with an average power gain of 15 dB for RF LNA [10], a fractional tuning range of 120% (0.7-2.7 GHz LTE band) and NF of 5 dB (a fair assumption for total NF of 9 dB for the wideband UE LTE receiver), a target FoM of 41 dBm is obtained. Assuming the slope of a trend line from Fig. 6, the expected increase in FoM is equal to +14.2 dB, corresponds to the required increase in power of +75 mW. Note that four of the reported LNAs [17,21,26,32] meet the FoM requirement, however either a bandwidth is smaller, IIP3 is inadequate or noise is to high (note that the authors usually present the best performance not the average over bandwidth) for an LTE system. A validity of the presented discussion can be confirmed by comparison to the state of the art commercial LNA chip ADL5521 from Analog Devices [10]. Although realised in GaAn pHemt technology (higher f_t and lower noise than CMOS), its performance follows the trend of FoM presented in this paper. The reported parameters are (averaged): NF=1 dB, G=15 dB, IIP3=21 dBm, FBW=163.6%, and calculated FoM is equal to 57 dB, that is +30.2 dB above the CMOS average presented in this paper. According to our prediction the LNA core should consume +159 mW more than the CMOS average, resulting in total of 177 mW. The reported value for ADL5521 is 300 mW from 5V supply, however the core power consumption is not disclosed (some of the reported power is used by active bias replica). Thus it can be seen, that in practice, high performance LTE LNAs are power hungry circuits, as showed in this paper.

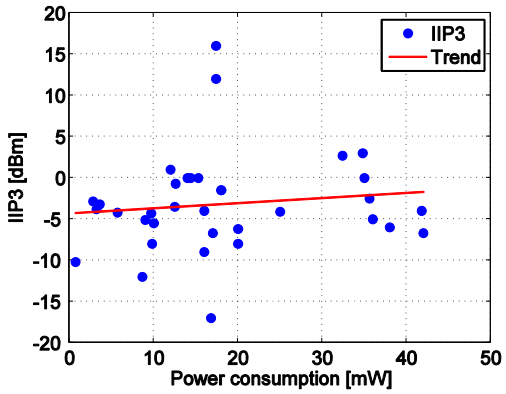

Fig. 5. Comparison of published LNA: IIP3 vs. power.

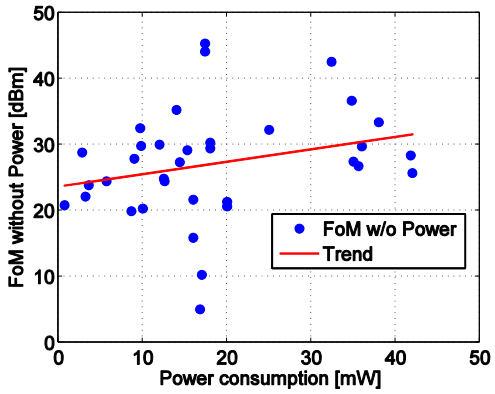

Fig. 6. Comparison of published LNA: FoM vs. power.

VI Conclusion

The presented results show that in general, LNA linearity as a standalone parameter is indirectly dependent on power. For a certain IIP3 performance, LNA circuit can be designed without increase in power, as indicated by Fig. 5. However, taking into account noise figure, gain and bandwidth constraints, more power has to be delivered to the amplifier, and hence, increasing LNA linearity levels will translate into higher power consumption. This is especially crucial for the wideband systems (LTE and beyond), where inadequate filtering leads to stringent intermodulation specifications, that in turn have significant impact on the power consumption for the whole receiver.

Table 3. Performance comparison of wideband CMOS LNA circuits.										
Ref.	**Year**	**CMOS**	**Gain**	**NF**	**f_{min}**	**f_{max}**	**FBW**	**IIP3**	**P_{DC}**	**FoM**
		[nm]	**[dB]**	**[dB]**	**[MHz]**	**[MHz]**	**[%]**	**[dBm]**	**[mW]**	**[dBm]**
[11]	2004	250	6.85	2.4	2	1600	199.5	0	35	**27.45**
[12]	2005	180	9.7	5	1200	11900	163.4	-6.2	20	**20.63**
[13]	2005	130	9.5	3.5	100	6500	193.9	1	12	**30.01**
[14]	2005	130	16	5.7	2000	5200	88.9	-6	38	**23.79**
[15]	2005	130	13	4	100	900	160	-10.2	0.72	**20.84**
[16]	2006	180	12.5	4.5	470	860	58.6	-4	16	**21.68**
[17]	2006	90	12.5	2.6	500	8200	177	-4	41.8	**28.38**
[18]	2006	90	12	2	500	7000	173.3	-6.7	42	**25.69**
[19]	2006	90	10	3.5	800	6000	152.9	-3.5	12.5	**24.85**
[20]	2007	90	8	5.3	400	1000	85.7	-17	16.8	**5.03**
[21]	2007	130	12.5	2.7	800	2100	89.7	16	17.4	**45.33**
[22]	2007	130	15.1	2.5	3100	10600	109.5	-5.1	9	**27.89**
[23]	2007	130	17	2.4	1000	7000	150	-4.1	25	**32.26**
[24]	2007	90	17.4	2.6	0	6000	200	-8	9.8	**29.81**
[25]	2007	65	15.6	3	200	5200	185.2	0	14	**35.28**
[26]	2008	180	20.5	3.5	20	1180	193.3	2.7	32.4	**42.56**
[27]	2008	90	16.5	2.7	0	6500	200	-4.3	9.7	**32.51**
[28]	2008	90	8	6	100	8000	195.1	-9	16	**15.90**
[29]	2009	180	10.5	3.5	300	920	101.6	-3.2	3.6	**23.87**
[30]	2009	130	7	3.7	1900	2400	23.3	-6.7	17	**10.27**
[31]	2009	180	14	3	48	1200	184.6	3	34.8	**36.66**
[32]	2009	65	16	5.5	800	5000	144.8	12	17.4	**44.11**
[33]	2009	65	16.5	3.9	1000	10000	163.6	-5	36	**29.74**
[34]	2010	180	8.45	3.2	1050	3050	97.6	-0.7	12.6	**24.44**
[35]	2010	130	9	2.5	100	5000	192.2	-8	20	**21.34**
[36]	2010	130	9.5	3.4	200	3800	180	-4.2	5.7	**24.45**
[36]	2010	130	7.5	4.1	200	3800	180	-3.8	3.2	**22.15**
[37]	2010	180	9.75	3	50	860	178	-2.5	35.6	**26.75**
[38]	2010	90	13.1	3.9	470	750	45.6	-5.5	10	**20.32**
[39]	2010	180	8.2	3.4	50	900	178.9	0	14.4	**27.33**
[40]	2011	90	10.5	1.7	2	2300	199.7	-1.5	18	**30.30**
[40]	2011	90	20	1.9	20	1100	192.9	-1.5	18	**29.45**
[41]	2011	90	11.5	2.35	100	1770	178.6	-2.85	2.8	**28.82**
[42]	2012	180	11.75	2.7	320	1000	103	0	15.3	**29.18**
[43]	2013	65	12	3	100	10000	196	-12	8.64	**19.92**

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REFERENCES

[1] http://www.3gpp.org, accessed April 2013.

[2] H. Holma and A. Toskala, "LTE for UMTS : OFDMA and SC-FDMA based radio access". Chichester, U.K: Wiley, 2009.

[3] P. Wambacq and W. Sansen, "Distortion Analysis of Analog Integrated Circuits". Boston: Kluwer Academic, 1998.

[4] B. Razavi, RF Microelectronics. Englewood Cliffs: Prentice Hall, 1998.

[5] T. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge: Cambridge University Press, 2004.

[6] H. Zhang, E. Sanchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," *Circuits and Systems I: Regular Papers, IEEE Transactions on* , vol.58, no.1, pp.22-36, Jan. 2011.

[7] S. Sesia, M. Baker and I. Toufik, "LTE, the UMTS long term evolution: from theory to practice". Chichester, U.K: Wiley, 2009.

[8] C. W. Liu and M. Damgaard, "IP2 and IP3 Nonlinearity Specifications for 3G/WCDMA Receivers", *High Frequency Electronics*, pp.16-29, Jun. 2009.

[9] http://www.avagotech.com, accessed April 2013.

[10] http://www.analog.com, accessed April 2013.

[11] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low noise amplifier exploiting thermal-noise cancelling", *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[12] C.-F. Liao and S.-I. Liu, "A Broadband Noise-Cancelling CMOS LNA for 3.1-10.6-GHz UWB Receiver", *in Custom Integrated Circuits Conference, Proceedings of the IEEE 2005*, pp. 161-164, Sept. 2005.

[13] S. Chehrazi, A. Mirzaei, R. Bagheri, and A. Abidi, "A 6.5 GHz wideband CMOS Low Noise Amplifier for Multi-Band Use", *in Custom Integrated Circuits Conference, Proceedings of the IEEE 2005*, pp. 801-804. Sept. 2005.

[14] R. Gharpurey, "A Broadband Low-Noise Front-End Amplifier for Ultra Wideband in 0.13-um CMOS", *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 9, pp. 1983-1986, Sept. 2005.

[15] S. B. T. Wang, A. M. Niknejad, and R. W. Brodersen, "A sub-mW 960-MHz ultra-wideband CMOS LNA", *in Proc. IEEE RFIC*, pp. 35–38, 2005.

[16] T. W. Kim and B. Kim, "A 13-dB IIP3 improved low-power CMOS RF programmable gain amplifier using differential circuit transconductance linearization for various terrestrial mobile D-TV applications", *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 945–953, Apr. 2006.

[17] J.-H.C. Zhan and S. Taylor, "A 5 GHz Resistive-Feedback CMOS LNA for Low-Cost Multi-Standard Applications", *in Solid-State Circuits Conference, Digest of Technical Papers. IEEE 2006*, pp. 721-730, Feb. 2006.

[18] B. G. Perumana, J.-H. C. Zhan, S. S. Taylor, and J. Laskar, "A 0.5–6GHz improved linearity, resistive feedback 90-nm CMOS LNA", *in Proc. IEEE Asian Solid-State Circuits Conf*., pp. 263–266, 2006.

[19] R. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M.Mikhemar, W. Tang, and A. A. Abidi, "An 800-MHz–6 GHz Software-defined wireless receiver in 90-nm CMOS", *IEEE J. Solid-State Circuits,* vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[20] M. Vidojkovic, M. Sanduleanu, J. van der Tang, P. Baltus, and A. van Roermund, "A 1.2 V, inductorless, broadband LNA in 90 nm CMOS LP", *in IEEE RFIC Symp. Dig.*, pp. 53–56, 2007.

[21] W.-H. Chen, G. Liu, B. Zdravko, and A. M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation", *in Proc. IEEE RFIC Conf. Dig.,* pp. 61–64, 2007.

[22] M. Reiha and J. Long, "A 1.2 V Reactive-Feedback 3.110.6 GHz Low-noise Amplifier in 0.13 um CMOS", *Solid-State Circuits, IEEE Journal of,* vol. 42, no. 5, pp.1023-1033, May 2007.

[23] R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4V 25mw Inductorless Wideband LNA in 0.13 m CMOS", *in Solid-State Circuits Conference, Digest of Technical Papers. IEEE 2007*, pp. 424-425, Feb. 2007.

[24] J. Borremants, P. Wambacq, and D. Linten, "An ESD-protected DC-to-6 GHz 9.7 mW LNA in 90 nm digital CMOS", *in Solid-State Circuits Conference, Digest of Technical Papers. IEEE 2007*, pp. 422-423, Feb. 2007.

[25] S. C. Baakmeer, E. A. M. Klumperink, B. Nauta, and D. M. W. Leenaerts, "An inductorless wideband balun-LNA in 65 nm CMOS with balanced output", *in Proc. ESSCIRC, 2007*, pp. 364–367, 2007.

[26] S. Seong-Sik, I. Dong-Gu, K. Hong-Teuk, and L. Kwyro, "A highly linear wideband CMOS low-noise amplifier based on current amplification for digital TV tuner applications", *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 118–120, Feb. 2008.

[27] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, "Low-Area Active-Feedback Low-Noise Amplifier Design in Scaled Digital CMOS", *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 11, pp. 2422-2433, Nov. 2008.

[28] T. Chang, J. Chen, L. Rigge, and J. Lin, "A packaged and ESD-protected inductorless 0.1–8 GHz wideband CMOS LNA", *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 6, pp. 416–418, Jun. 2008.

[29] S.Woo, W. Kim, C. Lee, K. Lim, and J. Laskar, "A 3.6mW differential common-gate CMOS LNA with positive-negative feedback", *in IEEE Int. Solid-State Circuits Conf. Tech. Dig., pp*. 218–219 Feb. 2009.

[30] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A CMOS low noise amplifier with reconfigurable input matching network", *IEEE Trans. Microw. Theory Tech.,* vol. 57, no. 5, pp. 1054–1062, May 2009.

[31] D. Im, I. Nam, H.-T. Kim, and K. Lee, "A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner", *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 686–698, Mar. 2009.

[32] W-H. Chen, "Designs of Broadband Highly Linear CMOS LNAs for Multiradio Multimode Applications", *PhD thesis*, Univ. of California, Berkley, August 2010.

[33] S. K. Hampel, O. Schmitz, M. Tiebout, and I. Rolfes, "Inductorless 1–10.5 GHz wideband LNA for multistandard applications", *in Proc. IEEE Asian Solid-State Circuits Conf.*, pp. 269–272, 2009.

[34] K. Jusung, S. Hoyos, and J. Silva-Martinez, "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization", *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 9, pp. 2340–2351, Sep. 2010.

[35] D. Im, I. Nam, J.-Y. Choi, B.-K. Kim, and K. Lee, "A CMOS active feedback wideband single-to-differential LNA using inductive shunt peaking for SAW-less SDR receivers", *in IEEE A-SSCC Tech. Dig.*, pp. 1–4, Nov. 2010.

[36] H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.

[37] D. Im, I. Nam, and K. Lee, "A CMOS active feedback balun-LNA with high IIP2 for wideband digital TV receivers", *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 12, pp. 3566–3579, Dec. 2010.

[38] P.-I. Mak and R. Martins, "A -enabled mobile-TV RF front-end with TV-GSM interoperability in 1-V 90-nm CMOS", *IEEE Trans. Microw. Theory Tech.,* vol. 58, no. 7, pp. 1664–1676, Jul. 2010.

[39] Y.-H. Yu, Y.-S. Yang, and Y.-J. Chen, "A compact wideband CMOS low noise amplifier with gain flatness enhancement", *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 502–509, Mar. 2010.

[40] M. El-Nozahi, A. A. Helmy, E. Sanchez-Sinencio, and K. Entesari, "An Inductor-Less Noise-Cancelling Broadband Low Noise Amplifier With Composite Transistor Pair in 90 nm CMOS Technology", *Solid-State Circuits, IEEE Journal of* , vol.46, no.5, pp.1111-1122, May 2011.

[41] E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari and E. Sanchez-Sinencio, "A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback", *Microwave Theory and Techniques, IEEE Transactions on* , vol.59, no.12, pp.3154-3161, Dec. 2011.

[42] M. Moezzi and M. S. Bakhtiar, "Wideband LNA Using Active Inductor with Multiple Feed-Forward Noise Reduction Paths", Microwave Theory and Techniques, IEEE Transactions on, vol.60, no.4, pp.1069-1078, April 2012.

[43] J. W. Park, B. Razavi, "A Harmonic-Rejecting CMOS LNA for Broadband Radios", *Solid-State Circuits, IEEE Journal of* , vol.48, no.4, pp.1072,1084, April 2013.